PULSE PATTERN GENERATOR
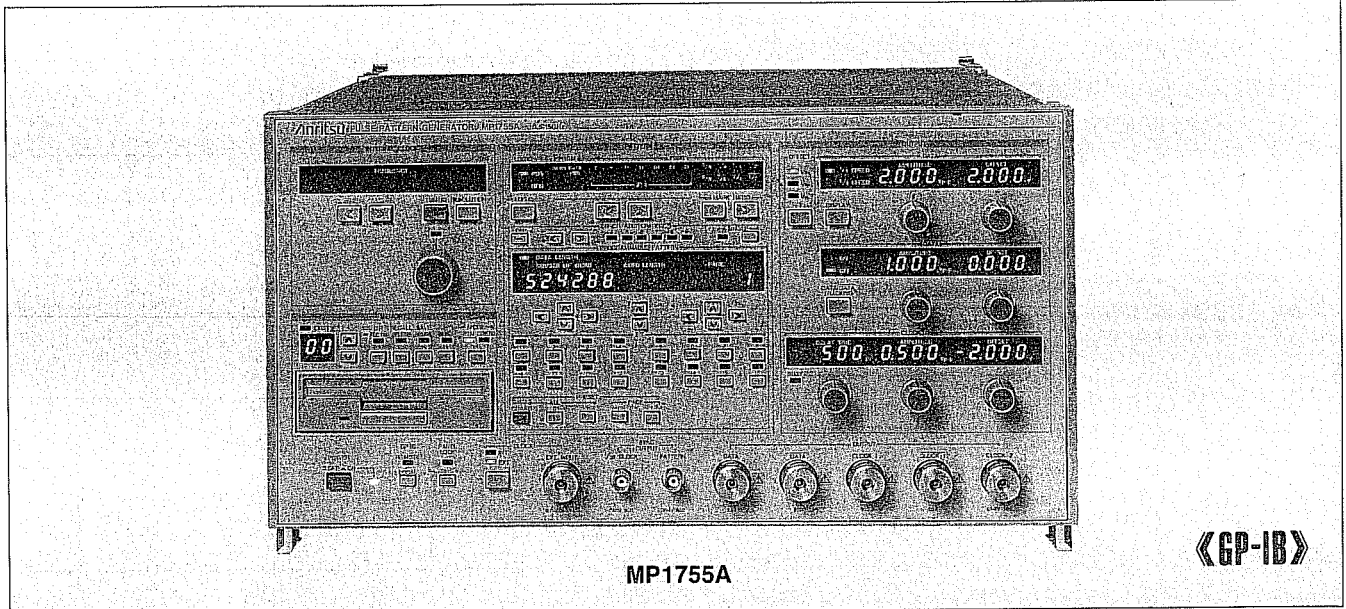# MP1755A, MP1763B, MP1652A
15 GHz   12.5 GHz   3 GHz
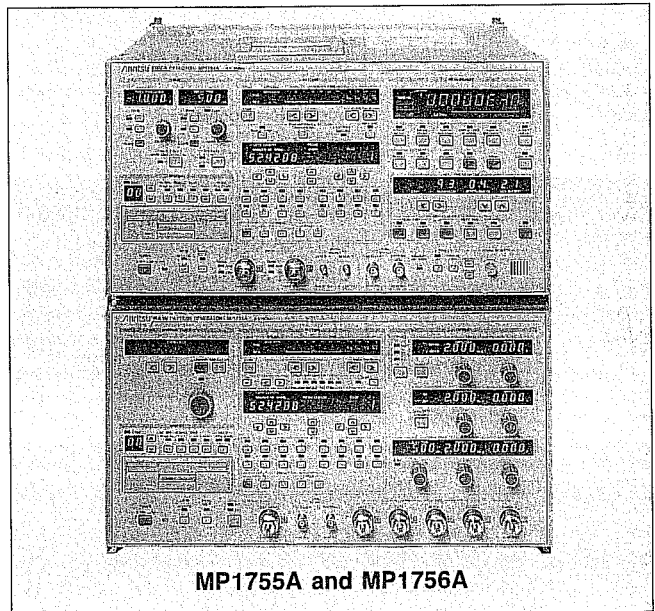

MP1755A   《GP-IB》

The MP1755A/1763B/1652A are used in combination with the MP1756A/ 1764A/1653A Error Detectors, respectively. The amplitude of the clock and data signals can be varied from 0.5 to 2 Vp-p (0.25 to 2 Vp-p, MP1763B) while the offset can be adjusted to within ±2 V. So that the amplitude and the offset margin can be measured. The clock has a variable delay function so that time-dependent characteristics or phase margins of the input clock and data can be measured for any instrument. An M series pseudorandom pattern representative of actual conditions or a programmable pattern can be selected as cell data.

In addition, a 3.5-inch floppy disk drive is built-in for storing preset data, enabling rapid measurements to be performed by simply pressing a key. A GP-IB function is provided, enabling automatic or remote measurement via an external controller.

The MP1755A/1763B/1652A are pulse pattern generators ideal for research and development of high-speed logic ICs and digital systems. The MP1755A needs an external signal source.

Features
- High quality waveform
- Low FM/PM-noise clock generator (except for the MP1755A)
- 8 Mbit programmable pattern corresponding to six frames of STM-64/ STS-192 (MP1763B)
- Generates PRBS patterns with bit length from $2^7 - 1$ to $2^{31} - 1$ bits
- Complementary outputs both data and clock
- The amplitudes and offsets of all 4 data outputs that have 1/4 speed of fundamental clock signal can be set (MP1763B is 1/8 speed 8 channel outputs and level fixed as standard, 1/4 speed outputs as option.)

MP1755A and MP1756A

Specifications

Model		MP1755A	MP1763B	MP1652A
Operation frequency	Internal clock	–	0.05 to 12.5 GHz (option)	0.05 to 3 GHz
	External clock	0.5 to 15 GHz	0.05 to 12.5 GHz	0.05 to 3 GHz
External clock	Input level	0.7 to 2.0 Vp-p	0.4 to 2.5 Vp-p	0.7 to 2.0 Vp-p
	Input waveform	Sinusoidal or square wave	Square wave with rise/fall time of less than 1 ns, duty factor 50% (0.05 to 0.5 GHz) Sinusoidal wave or square wave with rise/fall time of less than 1 ns, duty factor 50% (>0.5 GHz)	
	Input connector	APC-3.5		Precision N-type
Internal clock	Frequency range	–	0.05 to 12.5 GHz (option)	0.05 to 3 GHz
	Frequency setting resolution	–	1 kHz, 1 MHz	
	Stability	–	±1 ppm	
	SSB phase noise (at 10 kHz offset, 1 Hz bandwidth)	·	−85 dBc/Hz (0.05 to 4 GHz) −80 dBc/Hz (4 to 8 GHz) −75 dBc/Hz (8 to 10 GHz) −70 dBc/Hz (10 to 12.5 GHz)	−85 dBc/Hz (0.05 to 3 GHz)
	Reference signal	–	10 MHz (internal/external, selectable)	
Pattern	Pseudorandom binary sequence pattern (PRBS)	Pattern: 2^n-1 (n: 7, 9, 11, 15, 20, 23, 31) Mark ratio: 1/2, 1/4, 1/8, 0/8 (1/2, 3/4, 7/8, 8/8 are possible with logic inversion) Number of AND bit shift when setting mark ratio: 1, 3 bit (selectable by using DIP switch on rear panel)		
	Data pattern[*1]	Data length: 2 to 524288 bits (MP1755A, MP1652A), 2 to 8388608 bits (MP1763B) Pattern reset/preset: ALL/PAGE selectable		
	Word pattern[*1]	Word length: 2 to 16 bits Number of words: 1 to 32768 Pattern reset/preset: ALL/PAGE selectable	–	Word length: 2 to 16 bits Number of words: 1 to 32768 Pattern reset/preset: ALL/PAGE selectable
	External pattern input mode	Number of channels: 8 channels (1 to 8 external input channels can be set) Pattern bit rate: 1/8 of fundamental clock 1/8 clock output for external pattern generation: ECL, should be connected 50 Ω termination, connected to −2 V External pattern input level: ECL, 50 Ω termination, connected to −2 V Connector: SMA	–	Number of channels: 8 channels (1 to 8 external input channels can be set) Pattern bit rate: 1/8 of fundamental clock 1/8 clock output for external pattern generation: ECL, should be connected 50 Ω termination, connected to −2 V External pattern input level: ECL, 50 Ω termination, connected to −2 V Connector: SMA
	Logic inversion	Provided		
	Alternate pattern	–	A/B pattern data length: 128 to 4194304 (128 bit steps) Loop time: A, B pattern (1 to 127, 1 steps)	–
	Zero substitution pattern	–	Zero bit length: 1 to (pattern length −1) bits Pattern: 2^n (n: 7, 9, 11, 15)	–
	Error addition	Error rate: 10^{-n} (n: 4, 5, 6, 7, 8, 9), and single error Addition position (selectable with rear panel DIP switch): Possible to insert into any 1 CH of 32 CH (MP1755A, MP1763B), possible to insert into any 1 CH of 16 CH (MP1652A)		
Data output	Output waveform	NRZ		
	Number of output	2 (DATA/DATA)		
	DATA/DATA tracking mode	ON/OFF selectable		
	Amplitude	0.5 to 2 Vp-p, 10 mV steps (setting error: ±15% or ±100 mV, whichever is greater)	0.25 to 2 Vp-p, 2 mV steps (setting error: ±15% or ±100 mV, whichever is greater)	0.5 to 2 Vp-p, 10 mV steps (setting error: ±15% or ±100 mV, whichever is greater)
	Offset voltage	Voltage: −2 to ±2 V (VOH), 5 mV steps (setting error: ±15% of offset voltage, ±100 mV or ±15% of amplitude whichever is greatest Display: VOH, VTH or VOL selectable	Voltage: −2 to ±2 V (VOH), 1 mV steps (setting error: ±15% of offset voltage, ±100 mV or ±15% of amplitude whichever is greatest Display: VOH, VTH or VOL selectable	Voltage: −2 to ±2 V (VOH), 5 mV steps (setting error: ±15% of offset voltage, ±100 mV or ±15% of amplitude whichever is greatest Display: VOH, VTH or VOL selectable
	Rise/fall time	≦25 ps (20% to 80% of amplitude)	Typical 30 ps (10% to 90% of amplitude)	≦80 ps (10% to 90% of amplitude)
	Pattern jitter	See[*2]	≦20 psp-p, Typical 10 psp-p	≦20 psp-p
	Waveform distortion	≦10% or ≦100 mV whichever is greater	≦15% or ≦150 mV whichever is greater	≦10% or ≦100 mV whichever is greater
	Load impedance	50 Ω	50 Ω (with back termination)	
	Connector	APC-3.5		Precision N-type

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Model		MP1755A	MP1763B	MP1652A
Clock output	Number of outputs	3 (CLOCK 1, $\overline{\text{CLOCK 1}}$, CLOCK 2)		
	CLOCK delay	±500 ps (1 ps steps)		±1000 ps (2 ps steps)
	Amplitude (CLOCK 1, $\overline{\text{CLOCK 1}}$)	0.5 to 2Vp-p, 10 mV steps (setting error: ±15% or ±100 mV, whichever is greater	0.25 to 2 Vp-p (2 mV steps) Setting error: ±15% (1.5 to 2 Vp-p) ±25% (0.5 to 1.5 Vp-p) ±100 mV (0.25 to 0.5 Vp-p)	0.5 to 2 Vp-p, 10 mV steps (setting error: ±15% or ±100 mV, whichever is greater
	Amplitude (CLOCK 2)	2 Vp-p ±15% (fixed)	1 Vp-p ±35%	2 Vp-p ±15% (fixed)
	Offset voltage (CLOCK 1, $\overline{\text{CLOCK 1}}$)	Voltage: −2 to ±2 V (VOH), 5 mV steps (setting error: ±15% of offset voltage, ±100 mV or ±15% of amplitude whichever is the greatest) Display: VOH, VTH or VOL selectable	Voltage: −2 to ±2 V (VOH), 1 mV steps (setting error: ±15% of offset voltage, ±100 mV or ±15% of amplitude whichever is the greatest) Display: VOH, VTH or VOL selectable	Voltage: −2 to ±2 V (VOH), 5 mV steps (setting error: ±15% of offset voltage, ±100 mV or ±15% of amplitude whichever is the greatest) Display: VOH, VTH or VOL selectable
	Offset voltage (CLOCK 2)	0 V ±300 mV (VOH)	0 V ±200 mV (VOH)	0 V ±300 mV (VOH)
	Rise/fall time	≦25 ps (20% to 80% of amplitude)	Typical 30 ps (10% to 90% of amplitude)	≦80 ps (10% to 90% of amplitude
	Waveform distortion	≦10% or ≦100 mV whichever is greater	≦15% or ≦150 mV whichever is greater	≦10% or ≦100 mV whichever is greater
	Duty factor adjust function	Three items of CLOCK 1, $\overline{\text{CLOCK 1}}$, CLOCK 2 adjustable with semi-fixed resistor	CLOCK 1, $\overline{\text{CLOCK 1}}$ adjustable	Three items of CLOCK 1, $\overline{\text{CLOCK 1}}$, CLOCK 2 adjustable with semi-fixed resistor
	Load impedance	50 Ω	50 Ω (CLOCK 1, $\overline{\text{CLOCK 1}}$: with back termination)	50 Ω (with back termination)
	Connector	APC-3.5	APC-3.5 (CLOCK 1, $\overline{\text{CLOCK 1}}$) SMA (CLOCK 2)	Precision N-type
1/4 data and clock output*3	Number of outputs	DATA: 4, CLOCK: 1		
	Output level	0.5 to 1 Vp-p, 10 mV steps (setting error: ±15% or ±100 mV, whichever is greater)	0.5 to 2 Vp-p, 2 mV steps (setting error: ±15% or ±100 mV, whichever is greater)	0.5 to 1 Vp-p, 10 mV steps (setting error: ±15% or ±100 mV, whichever is greater)
	Offset voltage	Voltage: −1.5 to ±1.5 V (VOH), 5 mV steps (setting error: ±150 mV) Display: VOH, VTH or VOL selectable	Voltage: −1.5 to +1.5 V (VOH), 1 mV steps (setting error: ±15% of offset voltage or ±15% of amplitude or ±100 mV whichever is greatest) Display: VOH, VTH or VOL selectable	Voltage: −1.5 to ±1.5 V (VOH), 5 mV steps (setting error: ±150 mV) Display: VOH, VTH or VOL selectable
	Rise/fall time	≦200 ps (20% to 80% of amplitude)	≦150 ps (20% to 80% of amplitude)	≦500 ps (20% to 80% of amplitude)
	Data output jitter	≦100 psp-p		
	Waveform distortion	≦15%		≦200 psp-p
	Skew (DATA/DATA, DATA/CLOCK)	≦100 ps		≦200 ps
	Connector	SMA		
1/8 data, clock output*4		−	Number of outputs: DATA 8, CLOCK 1 Output level: ECL Connector: SMA	−
Sync. signal output	Number of outputs	Pattern: 1 (BNC connector) 1/2 clock: 1 (SMA connector) 1/32 clock: 1 (BNC connector)	1 (1/32 clock, fixed position pattern, or variable position pattern selectable	Pattern: 1 (BNC connector) 1/2 clock: 1 (SMA connector) 1/16 clock: 1 (BNC connector)
	Output level	Amplitude: 1 Vp-p ±20%, offset voltage: 0 V ±200 mV (VOH)		
External control		GPIB, IEEE 488.2		
Operating temperature range		5° to 35°C	0° to 50°C	0° to 50°C (however, 5° to 45°C applied for memory floppy disk)
Parameter memory		Media: 3.5-inch FD (2HD, 2DD) Format: MS-DOS (Rev. 3.1)*5 Content: Programmable pattern, and other parameters		
Power		AC*6 V ±10%, 50/60 Hz, ≦700 VA (MP1755A, MP1763B), ≦620 VA (MP1652A)		
Dimensions and mass		221H × 426W × 451D mm, <33 kg		

·1 Relationship between number of pages and items of word length, number of words and data length
·2 ≦40 psp-p (≧2 GHz); ≦50 psp-p or 50% of pulse width (<2 GHz), including every other bit jitter, 1/2 jitter is adjustable using semi-fixed variable resistor.
·3 Standard feature (MP1755A, MP1652A), Option (MP1763B)
·4 When the option 03 (1/4 speed output) is added, the 1/8 speed output is not available.
·5 The MP1755A/1652A cannot perform 2DD-type disk formatting. Please use a personal computer to format 2DD-type disks. MS-DOS is a registered trademark of Microsoft Corporation.
·6 Specify one nominal line voltage between 100 and 240 V when ordering. Maximum operating voltage is 250 V.

⊛ Numerical relation between word length and number of words (MP1755A/1652A)

Word length	Number of words		
	Per 1 step	Step width	Range
2	1 to 2048	64 step	2112 to 32768
3	1 to 1365	128 step	1408 to 32768
4	1 to 1024	32 step	1056 to 32768
5	1 to 819	128 step	896 to 32768
6	1 to 682	64 step	704 to 32768
7	1 to 585	128 step	640 to 32768
8	1 to 512	16 step	528 to 32768
9	1 to 455	128 step	512 to 32768
10	1 to 409	64 step	448 to 32768
11	1 to 372	128 step	384 to 32768
12	1 to 341	32 step	352 to 32768
13	1 to 315	128 step	384 to 32768
14	1 to 292	64 step	320 to 32768
15	1 to 273	128 step	384 to 32768
16	1 to 256	8 step	264 to 32768

⊛ Numerical relation between data length and step width (MP1755A/1652A)

Data length	Step width
2 to 4095	1 step
4224 to 524288	128 step

⊛ Numerical relation between data length and step width (MP1763B)

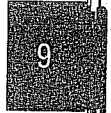| Data length	Step width
2 to 65536	1 step
66536 to 131072	2 step
131072 to 262144	4 step
262144 to 524288	8 step
524228 to 1048576	16 step
1048576 to 2097152	32 step
2097152 to 4194304	64 step
4194304 to 8388608	128 step

⊛ Relationship between pages of WORD mode and DATA mode

Output pattern/mode	Variable page range
WORD	1 word to the number of words that have been set, 1 step width
DATA	1 to < data length/16, 1 step width (Up to quotient value when the remainder is 0, up to quotient value +1, 1 step width) Data length : Number of page 2 to 16 : 1 17 to 32 : 2 33 to 48 : 3 ≧49 : ≧4

⊛ Floppy disk format (MP1755A/1652A)

Media type	Memory capacity	Sector length	Sector number	Track number	Recording surface
2HD	1232 Kbytes	1024 bytes	8	77	Double-sided
2DD	720 Kbytes	512 bytes	9	80	Double-sided

⊛ Floppy disk format (MP1763B)

Media type	Memory capacity	Sector length	Sector number	Track number	Recording surface
2HD	1440 Kbytes	512	18	80	Double-sided
2DD	720 Kbytes	512	9	80	Double-sided
2HD	1232 Kbytes	1024	8	77	Double-sided
2DD	640 Kbytes	512	8	80	Double-sided